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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,582	04/24/2001	Kazuo Nishiyama	09792909-4979	5398

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EXAMINER	
ZARNEKE, DAVID A	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	09/841,582	NISHIYAMA ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 11/23/04, with respect to the rejection of the claims have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made below.

Rejections using Farnworth, US Patent 5,933,713

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Farnworth, US Patent 5,933,713.

Farnworth (figure 7) teaches an electronic component comprising at least one semiconductor chip [20] having at least its electrodes formed exclusively on one surface

thereof (22), and surfaces other than said one surface are continuously covered with a protective material [50].

The limitation "wherein the protective material adjacent to side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent to the sides of the semiconductor chip" is a process limitation that defines a product-by-process claim. The process used to form the vertical side walls is irrelevant to the product. The structure defined by the claims must merely have vertical side walls, regardless of how they are formed.

Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

Regarding claim 2, Farnworth teaches the protective insulating material comprises an epoxy (7, 14+), which is an organic insulating resin or an inorganic material.

With respect to claim 3, Farnworth teaches a semiconductor chip diced from a wafer at a position of said protective material for mounting on a package substrate, wherein said electrode is formed on said one surface, which is a device surface, of said semiconductor chip, and both a side wall and a bottom surface of said semiconductor chip are covered with said protective material (figure 8).

As to claim 4, Farnworth teaches a solder bump [30] formed on said electrode.

Rejections using Paik, US Patent 5,879,964

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Paik et al., US Patent 5,879,964.

Paik (figure 5a) teaches an electronic component comprising at least one semiconductor chip [1] having at least its electrodes formed exclusively on one surface thereof, and surfaces other than said one surface are continuously covered with a protective material [7], and further wherein the protective material adjacent to side surfaces of the semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent to the sides of the semiconductor chip (abstract).

Regarding claim 2, Paik teaches the protective insulating material comprises an epoxy (4, 21+), which is an organic insulating resin or an inorganic material.

With respect to claim 3, Paik teaches a semiconductor chip diced from a wafer at a position of said protective material for mounting on a package substrate, wherein said electrode is formed on said one surface, which is a device surface, of said semiconductor chip, and both a side wall and a bottom surface of said semiconductor chip are covered with said protective material (figure 5a).

As to claim 4, Paik teaches a solder bump [9] formed on said electrode.

Claims 6-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Paik et al., US Patent 5,879,964.

Paik (figure 5a) teaches a pseudo wafer comprising a plurality of semiconductor chips each having at least their electrodes formed solely on one surface thereof, wherein interspaces between said chips and bottom surfaces thereof are continuously covered with said protective material, and the chips are bonded with each other and further wherein the protective material adjacent the side surfaces of each semiconductor chip is cut to provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chips.

In re claim 7, Paik teaches the protective material comprises an epoxy (4, 21+), either is one of an organic insulating resin and an inorganic insulating material.

Regarding claim 8, Paik teaches the plurality of semiconductor chips arrayed thereon are diced at a position of said protective material between said plurality of semiconductor chips and thereafter mounted on a packaging substrate such that the protective material adjacent the side surfaces of the semiconductor chip is cut to

provide substantially vertical side walls of protective material formed adjacent the sides of the semiconductor chip.

With respect to claim 9, Paik teaches a solder bump [9] formed on said electrode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Paik et al., US Patent 5,879,964, as applied to claim 1 above.

While Paik fails to explicitly teach the use of a plurality of different types of semiconductor chips integrated and bonded by said protective material, it is a mere matter of design choice to use different types of chips as opposed to a single type of chip. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art cited but not relied upon teaches either the state of the art or similar inventions but do not qualify as prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-F 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571)-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
January 26, 2005